REMARKS

The following is intended as a full and complete response to the Office Action dated February 23, 2009, having a shortened statutory period for response set to expire on May 23, 2009. Claims 1-28 are pending in the application. Applicants respectfully request reconsideration and allowance of all claims in view of the following remarks.

35 U.S.C. § 102(e) Rejections

Claims 1-11 and 13-28 are rejected under 35 U.S.C. § 102(e) as being anticipated by Van Hook (U.S. 6,342,892). These rejections are respectfully traversed.

Claim 1 recites the limitations of a Physics Processing Unit (PPU) that comprising a vector processor that is adapted to perform multiple, parallel floating point operations to generate physics data and a data communication circuit adapted to communicate the physics data to a host. Van Hook fails to teach or suggest these limitations.

Van Hook discloses a video game system having a central processing unit (CPU) and a coprocessor that handles audio and video signals through a signal processor. The coprocessor in Van Hook includes various sub-processors, such as a signal processor and a CPU interface. The signal processor includes a vector unit that is configured to execute audio and graphics tasks (see Van Hook, column 16, lines 7-11). The vector unit in Van Hook receives commands from the CPU interface and executes those commands only to process graphics and audio data (see col. 18, lines 1-7 of Van Hook). In contrast, the vector processor of claim 1 generates physics data.

More importantly, the vector processor of claim 1 performs multiple, parallel floating point operations to generate the physics data. Van Hook is very clear that the vector unit does not perform floating point operations, stating that "signal processor 400 has no floating point unit" (see col. 18, lines 58-59 of Van Hook). The fixed point operations are invoked using instructions that are reserved for floating point operations of a conventional processor's instruction set (see claims 13 and 31 of Van Hook). However, all of the operations performed by the vector unit taught by Van Hook are performed using fixed point operations, not floating point operations. Specifically, when the vector unit in Van Hook is configured to perform double precision computations, the fixed point format includes a 16 bit integer and a 16 bit fraction (see col. 26, lines 37-51

of Van Hook). Nowhere does Van Hook teach or suggest that the vector unit or any other unit within the signal processor is configured to perform multiple parallel floating point operations, as explicitly recited in claim 1.

As the foregoing illustrates, Van Hook fails to teach or suggest each and every limitation of claims 1 and 9. In particular, Van Hook fails to teach or suggest generating physics data and Van Hook fails to teach or suggest performing multiple, parallel floating point operations. Therefore, claim 1 and claims 2-8, dependent thereon, are in condition for allowance.

Claim 9 recites also the limitations of a vector processor that is adapted to perform multiple, floating point operations. Therefore claim 9 is allowable for at least the same reasons as allowable claim 1. Since claims 10-11 and 13-28 depend on claim 9, these claims are also in condition for allowance.

35 U.S.C. § 103(a) Rejections

Claim 12 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Van Hook in view of Intel (Intel PCI and PCI Express). These rejections are respectfully traversed.

Claim 12 recites the limitations of at least one data communications protocol of USB, USB2, Firewire, PCI, PCI-X, PCI_Express, and Ethernet. The combination of Van Hook and Intel fails to teach or suggest these limitations.

Intel discloses a physical interface and is completely silent regarding the generation of physics data. The Examiner relies on Intel only to teach the PCI and PCI-Express interfaces. Thus, Intel fails to cure the deficiencies of Van Hook set forth above.

As the foregoing illustrates, the combination of Van Hook and Intel fails to teach or suggest each and every limitation of claim 12 (or any of the other pending claims). Therefore, all of the pending claims are in condition for allowance over the references cited by the Examiner.

CONCLUSION

In conclusion, the references cited by the Examiner, alone or in combination, do not teach, show, or suggest the invention as claimed. Having addressed all issues set out in the office action, Applicants respectfully submit that the claims are in condition for allowance and respectfully request that the claims be allowed. If the Examiner has any questions, please contact the Applicants' undersigned representative at the number provided below.

Respectfully submitted,

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